IN THE CLAIMS:

Claims 1-24 (Canceled)

25. (Currently Amended) An integrated circuit, comprising:

transistors;

interconnects formed in dielectric layers located over the transistors that interconnect the transistors to form an operative integrated circuit; and

a thin film resistor device interconnected to the transistors, including:

a resistive layer located on a first dielectric layer;

first and second contact pads located atop the resistive layer; and

a second dielectric layer located ~~atop~~ on the resistive layer and the first and second contact pads.

26. (Original) The integrated circuit as recited in Claim 25 further including a first interconnect that contacts the first contact pad and a second interconnect that contacts the second contact pad.

27. (Original) The integrated circuit as recited in Claim 26 further including interconnect metallization structures wherein the first dielectric layer is located between the interconnect metallization structure and the resistive layer.

28. (Original) The integrated circuit as recited in Claim 27 wherein each of the first

and second interconnects contact an interconnect metallization structure.

29. (Original) The integrated circuit as recited in Claim 26 wherein the first and second contact pads each have a width that is about 3000 nm greater than a width of at least one of the first and second interconnects.

30. (Original) The integrated circuit as recited in Claim 26 wherein the first and second interconnects comprise aluminum.

31. (Original) The integrated circuit as recited in Claim 30 wherein the first and second interconnects comprise a titanium/titanium nitride/aluminum/titanium nitride stack.

32. (Original) The integrated circuit as recited in Claim 25 wherein the resistive layer includes tantalum nitride.

33. (Original) The integrated circuit as recited in Claim 32 wherein the resistive layer further includes tantalum pentoxide.

34. (Original) The integrated circuit as recited in Claim 25 wherein the first and second contact pads comprise a titanium/platinum stack.

35. (Original) The integrated circuit as recited in Claim 34 wherein the

titanium/platinum stack includes titanium nitride located there between.

36. (Original) The integrated circuit as recited in Claim 25 wherein the resistive layer has a thickness ranging from about 20 nm to about 80 nm.

37. (Original) The integrated circuit as recited in Claim 25 wherein the transistors form part of a complementary metal oxide semiconductor (CMOS) device, bipolar device or BiCMOS device.